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10/673,506	09/30/2003	Eric J. Strang	231753US6YA	1663

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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
SIEK, VUTHE	
ART UNIT	**PAPER NUMBER**
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/673,506	STRANG, ERIC J.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/673,506 and RCE with amendment filed on 10/26/2006. Claims 1-69 remain pending in the application.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).
Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-69 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-44, 1-58, 1-1-48, 1-78 and 1-62 of copending Application No. 10/673,138, 10/673,467, 10/673,501, 10/673,507, 10/673,583 and 10/673,583 respectively. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims refereed to a method performed by a semiconductor processing tool comprising inputting process data, inputting a first principles physical model, performing a first principles simulation and using the first principles simulation result except for using first principles simulation result: to determine a fault in the actual process as in the instant

application; to facilitate the actual process as in copending Application No. 10/673,138; to built an empirical model as in copending Application No. 10/673,467; as part of a data set the characterizes the actual process as in copending Application No. 10/673,501; to control the process as in copending Application No. 10/673,507; and using the virtual sensor measurement to facilitate the actual process as in copending Application No. 10/673,583. Since the claims include identical structures, they would been anticipated various functions are recited in the claims.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made

5. Claims 1-25, 32-56 and 63-69 are rejected under 35 U.S.C. 103(a) as being obvious over Sonderman et al. (6,802,045) in view of Kee et al. (5,583,780).

6. As to claims 1, 32, 63 and 66, Sonderman et al. teach substantially similar claimed invention of a method and apparatus for analyzing a process performed by a semiconductor processing tool (Fig. 1-8 and its description) comprising inputting process data relating to an actual process performed by the semiconductor processing tool (process control environment 180 receives data (process data relating an actual

process being by semiconductor processing tool) from the manufacturing environment 170, at least col. 3 lines 50-64; Fig. 1); inputting a first principles physical model relating to the semiconductor tool (simulation environment 210 that includes device physics model, process model and equipment model, at least see in col. 5; Fig. 3); performing a first principles simulation for the actual process being performed during performance of the actual process using the physical model to provide a first principles simulation result (simulation data output by a simulator 340 of Fig. 3; at least col. 7 line 7 to col. 9 line 51) in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed in order to simulate the actual process being performed (Fig. 1-5; col. 5-7; specifically Fig. 3 describes a simulator simulates device physics model to provide a first principles simulation data result; the device physics model 310, the process model 320 and the equipment model 330 perform the functions or conditions of the device, process, and equipment, respectively, during a particular manufacturing process, col. 5 lines 10-67; the process control environment 180 utilizes the simulation data received from the simulation environment 210 in order to make control parameter adjustment or modifications for controlling manufacturing processes, col. 5 lines 40-47; the device physics model 310 comprises components that can measure electrical characteristics of a semiconductor wafer being manufactured; the device physics model comprises components that emulate or measure growth of oxide film on a semiconductor wafer; the device physics model 310 comprises components that can model the chemical reactions that can take place one a semiconductor wafer being processed, the process model and equipment are described

(col. 5 lines 47-55); and using the first principles simulation result obtained during the performance of the actual process to determine a fault (error) in the process performed by the semiconductor processing tool (Fig. 1-8, col. 5-7; specifically the simulation environment 210 includes a process control interface 350 allowing the simulation environment 210 to perform feedback corrections during the manufacturing of semiconductor wafers, col. 5 lines 18-27; the simulation environment 210 determines any error due to variations in the components in the defined models; using this error data, the system 100 of Fig. 1 performs a predictive state analysis 750 and sensitivity analysis 760 of Fig. 7; performing the predictive state analysis comprising predictive how a certain component within one of the models 310, 320, 330 behaves in response to modifications to another component in any one of the models in order to determine an optimum component levels to be implemented during manufacturing processes, described in col. 8, lines 12-67). Sonderman et al. also teach simulating process task (actual process) to provide simulation data results to enhance manufacturing process (col. 6 lines 24-64). Specifically, Sonderman et al. teach the simulation environment included the above integrated physical model, process model and equipment is simulated by a simulator (Fig. 3). The teachings of the simulation environment that includes device physics model, process model and equipment model (Fig. 3, col. 5 lines 10-18, lines 47-55), clearly suggest that the models must include some equations that are used for computation in order to determine electrical characteristics, growth of oxide film, control parameters and temperature. Some of equations are described in column 9. Accordingly, Examiner believes that the simulation environment that includes a

physics model, process model and equipment model correspond to physics-based first principles model. The simulation environment comprises a process control interface that allows communications between the simulation environment to receive manufacturing data from the manufacturing environment which can be used by the simulation environment to perform feedback corrections during the manufacturing of semiconductor wafers. There is an interaction performance between these models (physical model, process model and equipment model). Therefore, any modifications to any one of the three models can be made and analyzed by the simulator. The process control environment (item 180 Fig. 1) utilizes the simulation data received from the simulation environment in order to make control parameter adjustments or modifications for controlling manufacturing processes. The physics model comprises components that emulate or measure growth of oxide film on a semiconductor wafer. The device physics model also comprises components that can model the chemical reactions that can take place on a semiconductor wafer being processed. The process model and equipment model are described (col. 5 lines 47-67). Thus, simulation Sonderman et al. do not teach the first principles physical model including a set of computer-encoded **differential equations.** Kee et al. teach modeling apparatus that include physical models that can be used to develop real-time control systems for a particular actual thermal system for processing a silicon wafer (Fig. 1-2, see summary). The modeling apparatus (physical models) include a set of computer-encoded differential equations of the physical model parameters to quickly account for spectrial-radiation effects used in design and real-time control systems (col. 7 lines 3-44; col. 5 lines 23-67; col. 6 lines 1-

67; col. 11 lines 14-67; col. 12 lines 1-67; Figs. 1-2). Columns 7-10 describe set of differential equations. Thus, the modeling apparatus includes set of differential equations (first principles physical model that includes set of differential equations) can be used with confidence to predict effects of various approximations in the radiation transport and to facilitate the design of actual thermal systems for processing a semiconductor wafer (col. 12 lines 29-41). With above expected results and motivation, integrating the differential equations as taught by Kee et al. in Sonderman's first principles physical model would have been obvious to practitioners in the art at the time the invention.

7. As to claims 2 and 33 Sonderman et al. teach directly inputting the data (input data, process, manufacturing data, input control parameters) relating to a process performed by the semiconductor processing tool from at least on the physical sensor and a metrology tool physically mounted on the semiconductor processing tool (Fig. 1, 7, col. 4-8).

8. As to claims 3-5 and 34-36, Sonderman et al. teach indirectly inputting the data relating to a process performed by the semiconductor processing tool from at least one of a manual input device and a database, inputting data recorded from a process previously performed by the semiconductor processing tool, inputting data set by a simulation operator (Fig. 1-3, col. 1, manual fashion and automated fashion, col.4-7).

9. As to claims 6-9 and 37-40, Sonderman et al. teach inputting data relating to at least one of the physical characteristics of the semiconductor processing tool and the semiconductor tool environment, data relating to at least one of a characteristic and a

result of a process performed by the semiconductor processing tool; inputting a spatially resolved model of the geometry (modified models) of the semiconductor processing tool; inputting fundamental equations necessary to perform first principles simulation for a desired simulation result (Fig. 1-3, col. 5-9).

10. As to claims 10-13 and 41-44, Sonderman et al. performing interaction concurrently between simulation environment (first principles simulation) and the semiconductor processing tool (Fig. 2); performing simulation environment (first principles simulation) and the semiconductor processing tool (Fig. 2); performing first principles simulation using the input data to set a boundary condition and an initial condition of the first principles simulation model (Fig. 3, col. 5-8).

11. As to claims 14 and 45, Sonderman et al. teach using the simulation result (simulation data, simulation data result) to detect a fault in the process performed by the semiconductor processing tool by comparing the first principles simulation result with the input data (col. 7, Fig. 5-7).

12. As to claims 15-19 and 46-50, Sonderman et al. teach a system having a network of interconnected resources to perform at least one of the process steps as recited in Claim 1; using code parallelization among interconnected computational resources to share the computational load of the first principles simulation; sharing simulation information among interconnected resources to determine the fault in the process performed by the simulation processing tool; distributing simulation results among the interconnected resources to reduce redundant execution of substantially similar first principles simulations by different resources; distributing model changes

among the interconnected resources to redundant refinements of first principles simulations by different resources (Fig. 1-3, computer code software is described in col. 9 starting line 58; col. 5-8).

13. As to claims 20-21 and 51-52, Sonderman et al. teach remote access (Col. 9 line 58 to col. 10 line 31). Note that a wide area network is art inherent.

14. As to claims 22 and 53, Sonderman et al. teach performing simulation utilizing a computer software code (Col. 9 line 58 to col. 10 line 31).

15. As to claims 23-25 and 54-56, Sonderman et al. teach using the first principles simulation result (simulation data set results) to classify a fault in the process performed by the semiconductor processing tool (col. 6, lines 1-35); calculating a set of perturbations solutions corresponding to the first principles simulation for input data to generate a profile data solutions to the first principles simulation, inputting the perturbation solutions to a multivariate analysis; inputting a difference between the first principles simulation result and the input data to the multivariate analysis; and utilizing the multivariate analysis to identify a correlation between the input data and the difference (defining variations into the components of defined models in order to simulate the effects of online manufacturing performance by the models; modified models) (col. 5-8).

16. As to claims 64-65, Sonderman et al. teach interaction between simulation environment, process control environment and manufacturing/processing environment (sharing computational load of the simulation, sharing simulation information among interconnected resources) (Fig. 1-3).

17. As to claims 67-69, the integrated physical model as taught by Sonderman et al. and Kee et al. corresponds to a first principles physical model as claimed as described in above rejection. The simulation environment included the above integrated physical model is simulated by a simulator (Fig. 3 of Sonderman). The simulation environment includes device physics model, process model and equipment model (Fig. 3, col. 5 lines 10-18). The simulation environment comprises a process control interface that allows communications between simulation environment to receive manufacturing data from the manufacturing environment which can be used by the simulation environment to perform feedback corrections during the manufacturing of semiconductor wafers. There is an interaction performance between these models (physical model, process model and equipment model). Therefore, any modifications to any one of the three models can be made and analyzed by the simulator. The process control environment (item 180 Fig. 1) utilizes the simulation data received from the simulation environment in order to make control parameter adjustments or modifications for controlling manufacturing processes. The physics model comprises components that emulate or measure growth of oxide film on a semiconductor wafer. The device physics model also comprises components that can model the chemical reactions that can take place on a semiconductor wafer being processed. These teachings correspond to providing for the first principles simulation a reuse of known solutions as initial conditions for the first principles simulation because the simulation data is reused as initial conditions for the simulation environment.

18. Claims 26-31 and 57-62 are rejected under 35 U.S.C. 103(a) as being obvious over Sonderman et al. (6,802,045) in view Kee et al. (5,583,780) in further view of Fatke et al. (US 2005/0016947).

19. As to claims 26-28 and 57-59, Sonderman et al. do not explicitly teach the multivariate analysis comprising a partial least square analysis; defining a set of loading coefficients, computing at least one of mean and standard deviation values. Fatke et al. teach these limitations including defining a correlation matrix in order to improve detection of a feature etch completion process during semiconductor manufacturing to thereby providing accurate and precise completion of an etch process (see abstract, Fig. 4, summary, 0051). Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to combine these teachings in to the system as taught by Sonderman et al. in order to provide an accurate and precise completion of a process during semiconductor manufacturing.

20. As to claims 29-31 and 60-62, Sonderman et al. attributing the difference between simulated results and input data to one input data using the correlation; using the simulation result to detect a fault comprising detecting a fault (error) in at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposit system, a rapid thermal processing system for thermal annealing and a batch diffusion furnace (examples described in col. 4; detecting a fault in at least one of a chemical vapor deposition system and a physical vapor deposition system (col. 4, 6, 7, 8).

Remarks

21. Examiner thanks applicants for long arguments. Mainly, Applicants argued that Sonderman et al. do not teach or suggest performing a first principles simulation for the actual process being performed during performance of the actual process using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed. Examiner disagrees. At least the teachings of Sonderman can be found in col. 7 line 7 to col. 9 line 51 (detailed description can be found in Fig. 1-9). Under 103 rejection, if the difference between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Examiner respectively submits that combined references (6,802,045 to Sonderman et al. and 5,583,780 to Kee et al., as a whole, teach a first principles physical model including a set of computer-encoded differential equations or performing first principles simulation for the actual process being performed. From the disclosure as a whole, Sonderman et al. teach a simulation environment that includes device physics model, process model and equipment model (Fig. 3, col. 5 lines 10-18, corresponding to a first principles physical model). The device physics model comprises components that can measure electrical characteristics of a semiconductor wafer being manufactured. The device physics model also comprises components that emulate or measure growth of oxide film on a semiconductor wafer. The device physics model also comprises components that can

model the chemical reactions that can take place on a semiconductor wafer being processed (col. 5 lines 48-55). The process model and the equipment model are described (see col. 5 lines 56-67). These models clearly suggest that they must include some equations that are used for computation in order to determine electrical characteristics, growth of oxide film, control parameters and temperature. Some equations have been described (col. 9). Accordingly, Examiner believes that the simulation environment that includes a physics model, process model and equipment model correspond to physics-based first principles model. The Sonderman et al. does not teach the simulation environment (first principles physical model) including differential equations. Kee et al. teach, as a whole, modeling apparatus that include physical models that can be used to develop real-time control systems for a particular actual thermal system for processing a silicon wafer (Fig. 1-2, see summary). The modeling apparatus (physical models) include a set of computer-encoded differential equations of the physical model parameters to quickly account for spectrial-radiation effects used in design and real-time control systems for processing a silicon wafer of a semiconductor device (col. 7 lines 3-44; col. 5 lines 23-67; col. 6 lines 1-67; col. 11 lines 14-67; col. 12 lines 1-67; Figs. 1-2). Columns 7-10 describe set of differential equations. Thus, the modeling apparatus includes set of differential equations as taught by Kee (first principles physical model that includes set of differential equations) can be used with confidence to predict effects of various approximations in the radiation transport and to facilitate the design of actual thermal systems for processing a semiconductor wafer (col. 12 lines 29-41). With above expected results and motivation,

integrating the differential equations as taught by Kee et al. in Sonderman's first principles physical model would have been obvious to practitioners in the art at the time the invention considering the teachings as a whole from the cited references. The combined teachings, as a whole, render the claim limitation of first principles physical model including a set of computer-encoded differential equations obvious to practitioners the art at the time the invention was made. Examiner disagrees with Applicants that argued that Sonderman does not teach or suggest a first principles simulation for the actual process being performed. Sonderman et al. teach simulating the simulation environment (integrated physics model, process model and equipment model) (Fig. 3). It is common knowledge to practitioners in the art to recognize that performing the simulation environment (a first principles simulation) is performing the simulation environment for the actual process being performed. **Sonderman et al. clearly describes that the device physics model also comprises components that can model the chemical reactions that can take place on a semiconductor wafer being processed** (col. 5 lines 47-55). These cited portions as taught by Sonderman et al. clearly teach the claim limitation of performing first principles simulation for the actual process being performed. Also, Examiner has interpreted the cited portion description by applicants (col. 7 lines 14-18 of Sonderman) different way from Applicants. The cited portion recited "the **defined models** (simulation environment that includes physics model, process and equipment model) **can perform a simulation as if an actual manufacturing process were being performed**" (col. 7 lines 14-18). Examiner interpreted that portion as performing the defined models (simulation environment that

includes physics model, process model and equipment model corresponding to first principles simulation) as performing first principles simulation for the actual process being performed because the simulation imitates the actual process being performed. This is the fact of simulation performance. Practitioners in the art would recognize that performing a simulation model imitates the actual process being performed. In addition, Sonderman et al. teach the device physics model comprises components that can measure electrical characteristics of a semiconductor wafer being manufactured. The device physics model also comprises components that emulate or measure growth of oxide film on a semiconductor wafer. **The device physics model also comprises components that can model the chemical reactions that can take place on a semiconductor wafer being processed** (col. 5 lines 48-55). These teachings clearly suggest that when the simulation environment is simulated by a simulator (Fig. 3), the simulation environment being performed imitates the actual process being performed. Accordingly, Examiner believes that Sonderman et al. teach performing first principles simulation for the actual process being performed. Regarding to provisional double patenting, Examiner acknowledges that Applicants will file terminal disclaimers upon indication of allowance subject matter. However, there is no indication of allowable subject matter of the present claims at this time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe **Siek**

VUTHE SIEK
PRIMARY EXAMINER